

REMARKS

Claims 1-8 are pending. By this Amendment, claims 1, 3 and 4 are amended and Figures 1-2(e) are replaced. The drawings are revised to address the objection to the figures captions. The replacement sheets include larger figure captions. Reconsideration and withdrawal of the objection to the figures are respectfully requested. No new matter is added. Reconsideration in view of the above-outlined amendments and the following remarks are respectfully requested.

Claims 1 and 5 were rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 6,451,667 to Ning. This rejection is respectfully traversed.

Ning discloses a semiconductor wafer 100 having a workpiece 112, which may include a semiconductor substrate. An insulating layer 122 comprising an inter level dielectric is deposited over the workpiece 112. The insulating layer 122 is patterned, etched, and filled with a conductive material to form first conductive lines 124. The conductive lines 124 are preferably spaced apart to allow the formation of second conductive lines 136. A dielectric cap layer 126 is deposited over the insulating layer 122 and first conductive lines 124. A photoresist 128 is then applied to cover cap layer 126. A lithography mask is used to pattern the photoresist 128 to define the shape, size and location for the second set of conductive lines 136. The wafer 100 is then exposed to a UV light and developed to remove undesired portions of photoresist 128 leaving photoresist portions, which reside over portions of the insulating layer 122. Ning discloses etching the wafer 100 is etched to create trenches 130 abutting first conductive lines 124. Regions 132 of the insulating layer 122 may be between some of first conductive lines 124. A capacitor dielectric layer 134 is deposited over the first conductive lines 124, the regions 132 and trenches 130. A conductive material 136 is then deposited over the capacitor dielectric 134. The excess conductive material 136 is then removed from the surface to leave second conductive lines 136.

By contrast, amended claim 1 is directed to a method of fabricating a thin film capacitor. The method includes forming an interlayer insulating film over an entire surface of a semiconductor substrate. A first via and a second via is formed in the interlayer insulating film. The vias are spaced a predetermined distance from each other and are formed by selectively etching the interlayer insulating film. The first via and the second via are filled with a first metal material. The first material is planarized by chemical mechanical polishing to expose the interlayer insulating film such that the first via and the second via remain filled

IN THE DRAWINGS:

The attached sheets of drawings include changes to Figures 1, 2a, 2b, 2c, 2d, 2e, whereby the size of the figure captions has been enlarged. These sheets replace the original sheets showing Figures 1, 2a, 2b, 2c, 2d, 2e.

Attachment: Replacement Sheets

with the first metal material. The opposing surfaces of the first metal material in the first via and the second via are contacted by the interlayer insulating film. A capacitor window is formed by etching the interlayer insulating film the entire predetermined distance between the first via and the second via to have a predetermined depth such that the semiconductor substrate is exposed in the capacitor window. One surface of the first metal material in the first via remains in contact with the interlayer insulating film. One surface of the first metal material in the second via remains in contact with the interlayer insulating film. A dielectric layer is formed on an inner wall of the capacitor window and the exposed semiconductor substrate. A second metal material is fills in the capacitor window.

Ning does not anticipate the subject matter of amended to claim 1. In particular, Ning fails to disclose, teach or suggest that the first material located within the first via and the second via is planarized by chemical mechanical polishing to expose the interlayer insulating film such that the first via and the second via remain filled with the first metal material. Furthermore, Ning does not disclose forming a capacitor window by etching the interlayer insulating film the entire distance between the first via and the second via such that the first metal is exposed. As shown in Figure 4 in Ning, portions 132 of the insulating layer 122 remain between the conductive lines 124. Additionally, Ning does not disclose etching the insulating film to expose the semiconductor substrate in a capacitor window. There is no disclosure in Ning of exposing the substrate. Furthermore, Ning does not disclose that one surface of the first metal material in the first via remains in contact with the interlayer insulating film and one surface of the first metal material in the second via remains in contact with the interlayer insulating film. As shown in Fig. 4 in Ning, the conductive lines 124 are exposed on both sides such that they do not contact the insulating layer. Since Ning does not disclose exposing the semiconductor substrate in a capacitor window, Ning also does not disclose forming a dielectric layer on an inner wall of a capacitor window and the exposed semiconductor substrate. Ning does not disclose lining a cavity in such a manner. Applicants respectfully submit that Ning fails to anticipate the subject matter of the method of claim 1.

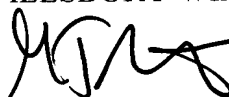
Accordingly, applicant respectfully submit that claim 1 is allowable over Ning. Claim 5 depends from claim 1 and is allowable over Ning for at least the same reasons. Reconsideration and withdrawal of the rejection are respectfully requested.

Claims 2-4 and 6-8 were rejected under 35 U.S.C. § 103(a) over Ning. This rejection is respectfully traversed.

Claims 2-4 and 6-8 depend, either directly or indirectly, from claim 1. As discussed above, Ning fails to disclose, teach or suggest the method of claim 1. Accordingly, applicant respectfully submits that claims 2-4 and 6-8 are allowable over Ning for at least the same reasons. Reconsideration and withdrawal of the rejection are respectfully requested.

Applicant respectfully submits that the claims define subject matter that is patentable over the prior art of record. Should any issues require further resolution, the Examiner is requested to telephone applicant's undersigned attorney to discuss and resolve these issues. Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,
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